Study the Effect of annealing temperature on the Structure of a-Se and Electrical Properties of a-Se/c-Si Heterojunction

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Abstract

In this work Study effect of annealing temperature on the Structure of a-Se and electrical properties of a-Se/c-Si hetrojunction have been studied.The hetrojunction fabricated by deposition of a-Se film on c-Si using thermal evaporation.

Electrical properties of a-Se/ c-Si heterojunction include I-V characteristics, in dark at different annealing temperature and C-V characteristics are considered in the present work.

C-V characteristics suggested that the fabricated diode was abrupt type, built in potential determined by extrapolation from $1/C^2$-V curve. The built - in potential (Vb_i) for the Se/ Si System was found to be increase from 1.21 to 1.62eV with increasing of annealing temperature.

Keywords
PSi/Si structure

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دراسة تأثير التلدين على الخواص التركيبية للسيلنيوم العشوائي والكهربائية للمفرق الهجيني a-Se/c-Si

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الخلاصة:

في هذا البحث تم دراسة تأثير التلدين على الخواص التركيبية للسيلنيوم والخواص الكهربائية للمفرق ألهجيني a-Se/c-Si الناتج من ترسيب السلنيوم بطريقة التبخير الحراري على السليكون.

الخواص الكهربائية للمفرق الهجيني تتضمن خصائص التيار–فولتية في حالة الظلام وبدرجات تلدين مختلفة وخصائص سعة –فولتية .

من خصائص سعة –فولتية تبين ان المفرق الهجيني هو من النوع الحاد وان جهد البناء تم حسابه من منحني الفولتية ومقلوب مربع السعة وتبين ان جهد البناء للمفرق الهجيني يزداد من 1,21 الى 1,62الكترون فولت بزيادة التلدين.

Introduction

IV-VI semiconductors are commonly considered to be promising materials for optoelectronic, applications, [1].TheIV-VI layers (chalcogenides) on Si substrates applications in the mid-infrared as optoelectronic emitters, sensors, and detectors.[2,3]

Recently, high-quality epitaxial growth of Se and related materials on (111) oriented Si substrates has been accomplished by incorporating thin intermediate BaF2/CaF2 layers. 1, 2 Heteroepitaxial growth of Se on silicon[4].This takes advantage of silicon integration technology to obtain inexpensive photonic devices. The Se layers that grown heteroepitaxially on Si(111) have been fabricated [5]. In this paper we will present a deposition a-Se thin film fabricated by the thermal evaporation technique. The preliminary results of structural and electrical properties of this alloy film have been presented.

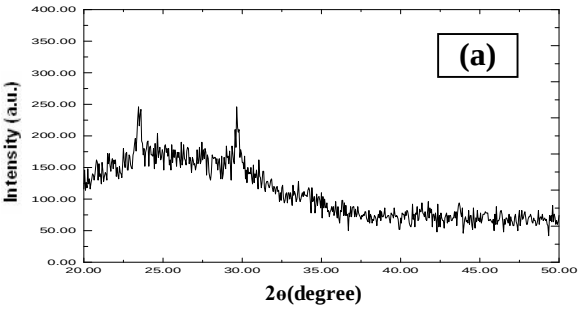
Experimental Work

Substrates of *n*-type single crystal Si wafers of resistivity 3(Ω-cm)
and orientation (111) were used in the present study. After scribing these wafers into small pieces (typically 1cm x 0.6cm in size), with one surface polished with 2HF: $3HNO_3$: $3CH_3COOH$ mixture (3:5:3) were cleaned ultrasonically by dipping in distilled water, acetone and isopropyl alcohol alternately. After cleaning, the samples were oxidized in dry oxygen [6]. The films of a-Se were prepared by thermal evaporation under vacuum of the order of 10^{-5}torr.The arate of evaporation was ≈0.8 nm/min, onto clean silicon mirror-like side substrates at room temperature (~300K). The average thicknesses of the deposits were determined by microbalance method. The maximum error in the determination of thickness was of the order of 10% estimated for the thinnest films (Se/Si films of thickness 350 nm). Ohmic contacts of Al Study on the electrical properties Se/Si Heterojunction aluminum [8] were evaporated on the silicon side and Se/Si side.

Results And Discussions

1-A X-ray Diffraction Studies

X- ray diffraction (XRD) studies have been carried out to identify the Se phase present in the film. Fig.1 shows the XRD pattern recorded on Se film, we can see XRD analysis are polycrystalline phase for all films. The XRD patterns of selenium films with annealing temperature Ta=323exhibit a prominent reflection angle 2ɵ=23.5192^o and 2ɵ=29.7133^o and and Ta=348K323exhibit a prominent reflection angle 2ɵ=23.5867^o and 2ɵ=29.7198^o



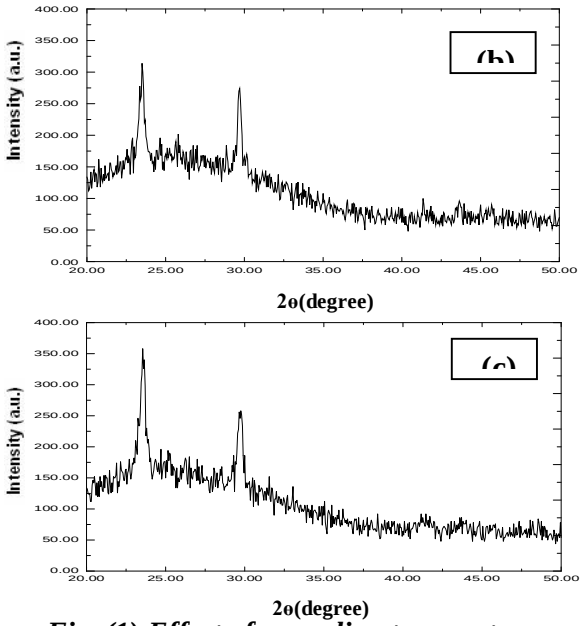
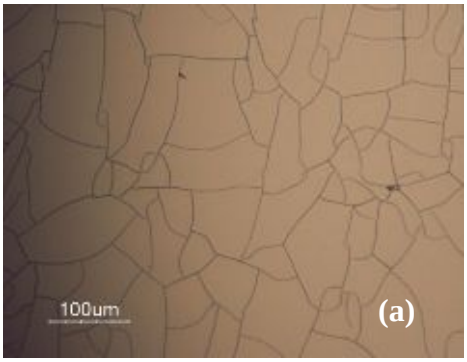
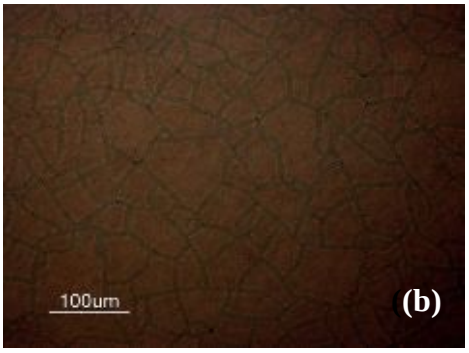


Fig. (1):Effect of annealing temperature on the XRD spectrum for Se coated glass substrate a-annealing temp.(R.T) b-annealing temp.(323K) c-annealing temp.(358K)

1- B Surface morphology

The locally amplified optical microscope (OM) image of the ternary a-Se films shown in fig. 2(a-c), which indicates that most of the films are straight with a uniform width of several micrometers . Their length can be extended to more than several hundreds of micrometers Morphology and surface roughness of a-Se films change significantly. When Increase in annealing (from RT to 348 K) increases the nucleation density of the crystals rather than the growth of already nucleated ones.





Fig(2):Effect of annealing on the Structure of Se a-annealing temp(R.TK) b-annealing temp(323K) c-annealing temp(358K)

2- I-V characteristics

The (I-V) characteristic shown in fig.(4).This illustrated in dark, for forward and reverse bias of p-Se/*n*-Si heterojunction is shown in Fig.3. In the forward bias the current increased exponentially with voltage as expected. But in reverse bias, the current was found to be increasing slowly with voltage (soft breakdown) and did not show any trend of saturation or sharp breakdown. This could be due to the domination of edge leakage current which is caused by the sharp edge at the periphery of the contact and also due to the generation of excess carriers in the depletion region at higher fields.

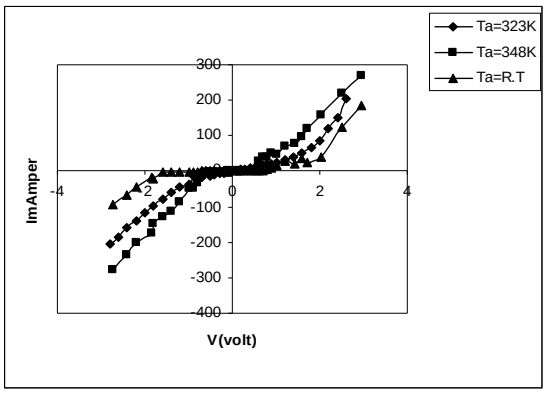


Fig. (3): I-V characteristics in the dark for p-Se/n-Si heterojunction atdifferent annealing temperature

The electrical properties of p-Se/n-Si heterojunction forward-bias region could be explained by an equation of the form [$J \approx exp\ (eV/\eta kT)$] and at the high-bias region by the equation, [$J \approx exp\ (Av)$] where η is a constant of the order of (2-6), and A is another constant, of the order of (13-14.5).This practically independent of temperature. Further analysis of these current characteristics with temperature shows that ln J varies approximately as -1/T in the high-biaregion: in the high-bias region,

ln J.

From this figure one can see that the high value of saturation current J_s . This may be originated of amorphous structure for good lattice defect and interface state at junction between a-Se and c-Si.

3-C-V Characteristics

The junction capacitance measured as a function of bias voltage for the *p*- Se/*n*-Si diodes shows $C \propto V^{-1/2}$ dependence. Fig.(5) which indicates an abrupt junction in that case. According to the distances during which the transition from one region to the other is completed near the interfaces. Under these conditions, the C-V characteristics of the heterojunction can be explained on the basis of Anderson's model [10], according to which

$$\frac{C}{a}=\left[\frac{qN_{A1}N_{D2}\varepsilon_1\varepsilon_2}{2(\varepsilon_1 N_{A1}+\varepsilon_2 N_{D2})}\cdot\frac{1}{V_D-V}\right]^{\frac{1}{2}} \quad ..(1)$$

where q is the electronic charge, ε_1 and N_{A1} are dielectric constant and concentration of donors in *n*-type semiconductor, ε_2 and ND_2 are dielectric constant and concentration of acceptors in *p*-type semiconductor (i.e. Si) respectively and V and V_D are the applied bias and built-in is voltage, respectively. Value of V_D estimated from $1/C^2$ versus V plot that obtained for heterojunction, the built - in potential (Vb_i.) for the p-Se/n-Si system was found to be increase with increasing of annealing temperature.

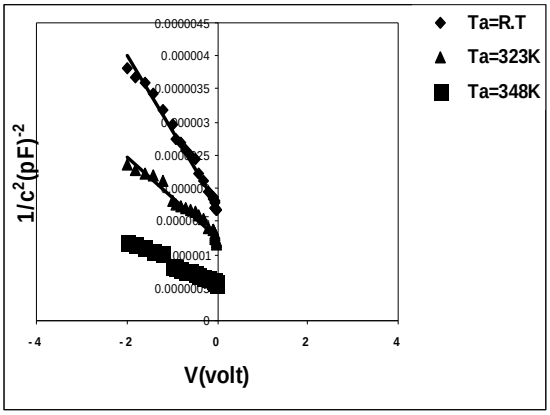


Fig.(4): 1/C2 as a function of reverse bias voltage and at different annealing temperature

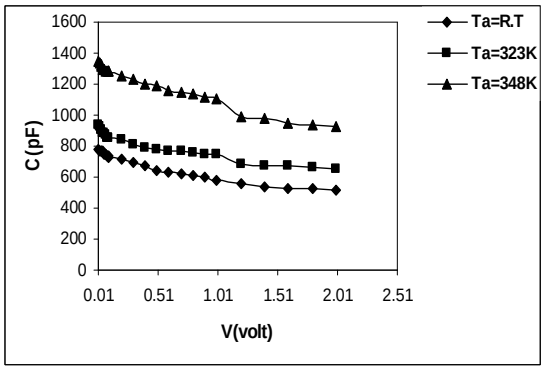


Fig.(5):The variation capacitance with voltage for Se/Si hetrojunction at different annealing

Table (1):Values of Vbi for Se/Si hetrojunction with annealing temperature

Annealing Temp (K)	Vbi(eV)
R.T	1.21
223	1.34
258	1.62

Conclusion

From what has been mentioned above, We can conclude that this type of p-Se/*n*-Si heterojunction behaves as a poor rectifier due to the interface state between a-Se and c-Si.

The junction is abrupt type and the built - in potential (Vb_i.) for the p -Se/n-Si System was found to be increase with increasing of annealing temperature.

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