Electrical Investigation of PSi/Si (n-type) structure

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Abstract

In this work, porous Silicon structures are formed with photochemical etching process of n-type Silicon(111) wafers of resistivity (0.02 Ω.cm) in hydrofluoric acid (HF) of concentration (39%wt) under light source of tungeston halogen lamp of (100 Watt) power. Samples were anodized in a solution of 39%HF and ethanol at 1:1 for 15 minutes. The samples were realized on n-type Si substrates Porous Silicon layers of 100µm thickness and 30% of porousity. Frequency dependence of conductivity for Al/PSi/Si/Al sandwich form was studied. A frequency range of 10^2-10^6Hz was used allowing an accurate determination of the impedance components. Their electronic transport parameters were determined using complex impedance measurements. These measurements provide a powerful tool for interpretation of basic properties such as the dielectric constant, polarizibility and frequency dependence in the crystallites and trapping mechanisms. The electrical conductivity is mainly controlled by hoping transport on localized states in the chaotic porous structure.

Keywords

PSi/Si structure

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الاستقصاء الكهربائي لم ركب PSi/Si (نوع n)

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الخلاصة

في هذا البحث تم تحضير السيليكون المسامي بطريقة الضوئي-الكيميائي لشرائح السيليكون((orientation (111) (n- type ومقاومية (0.02 Ω.cm) في حامض الهيدروفلوريك (HF) وبتركيز (39%) وباستخدام مصباح الهالوجين وبقدرة (100 watt) تم وضع العينات في سائل مكون من حامض الهيدروفلوريك والايثانول وبنسبة ١:١ ولمدة ١٥ دقيقة. العينات التي حضرت بهذه الطريقة كانت بسمك ١٠٠ مايكرون ومسامية ٣٠%. تم دراسة اعتمادية التوصيلية على التردد وعلاقتها مع الممانعة وللعينات المحضرة بشكل سندويج Al/PSi/Si/Al وضمن مدى الترددات(١٠^٢-١٠^٦ Hz) . تم دراسة الانتقالات الالكترونية والتي تم من خلالها حساب ثابت العزل والاستقطابية واعتماديتهما على التردد على ميكانيكية القنص في المواد البلورية. اما التوصيلية الكهربائية تم تفسيرها اعتمادا على ميكاتيكية القفز في المستويات الموضعية في التركيب العشوائي للسيليكون المسامي.

Introduction

Porous silicon (PS) materials are under intense investigation for optoelectronics application. The development of these materials is of commercial interest as they are compatible with IC fabrication, and their ability to be integrated into microelectronic silicon based technologies will allow production of low cost optoelectronics component and systems [1,2].

There are different morphologies depending on the initial type of silicon and the preparation. Nano porous form (crystallite size around 1-3 μm) was widely studied since more than 10 year particularly in the hope of silicon based photo-emitting devices production. Since few years, studies are devoted to other application [3] such as active layers for chemical sensors, insulating substrates [4, 5, 6] for thermal microsensors and passive optical devices.

We consider the case of amorphous PS. We finding review other prediction for the existence of self-trapped excitons, the radiative and non-radiative recombination rates and finally the dielectric properties of such crystallites.

The experiments based on the frequency dependence and the thermal activation of the conductivity give interesting data on the electrical transport parameter. Porous silicon (PS) is a composite of silicon residuals and empty pores. The nature of silicon nanocrystallites as a confined system should affect the dielectric response of PS [7].

Experimental

Silicon substrates are high quality single crystals nearly defect free, with a very low volume density of impurities and controlled amount of dopants [8]. Samples used in this study are (c-Si) wafer Si (111) orientation. (thickness 525μm and resistively (0.02 Ω.cm).The porous samples were then prepared by photochemical etching process in a solution of hydrofluoric acid (HF) 39% and ethanol (1:1) with etching time 30 minutes and optical power density(30 mW/cm^2).

Aluminum films were evaporated onto the PS layers for preparation of Al/PS/c-Si/Al sandwich structures (as shown in Fig.1) with (250nm) layer of Aluminum by means of thermal evaporation methods (using Edward type E306 A unit) .

For Ac measurements, an HP-RLC unit model (4275A) multifrequency meter has been used 100-400kHz with an accuracy of 0.1% Ac instrument is shielded by the copper sheet to avoid the distortion signal, and to prohibit the connectors among the experimental portion from becoming a source of noise by using coaxial cables and BNC connectors were used.

The amplitude of measuring Ac signal was kept law at 0.08 volt to avoid possible non linearity and instability [9,10].

It should mention here all electrical measurements were established in dark room.

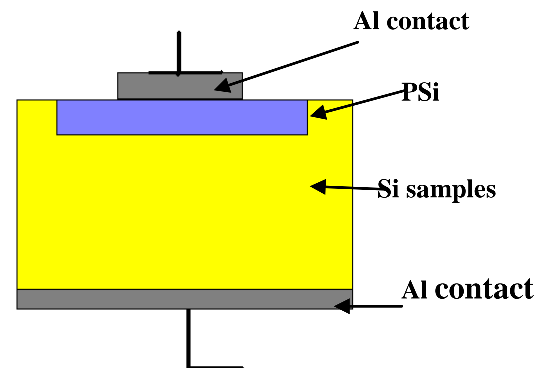


Figure (1): Configuration for the electrical measurements

Results and discussion

Figure (2) shows the structure of PS/Si(n-type) structure. There are several parameters affected on porous preparation such as etching time, HF concentration and light source intensity etc.., in this work it has been fixed all parameters at conditions as mentioned in experimental work, the porosity can be determined by weight measurements (Gravimetric method) by using the equation (1) [10,11]:

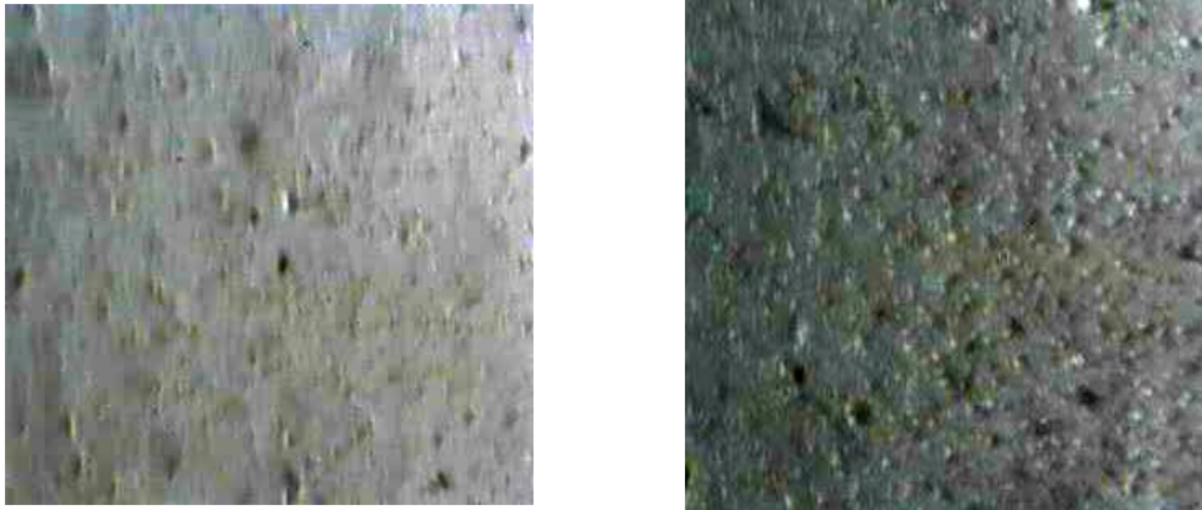


Fig. (2): Optical microscopy of porous Si n-type

$r=M_1-M_2/M_1-M_3$..............(1)

Where r is porosity, M_1 and M_2 are the weights of wafer Si before and after etching, M_3 is the weight of wafer Si after removing porous layer by KOH solution. The thickness of porous Silicon for light power density (30mW/cm2) at irradiation time (30min) is equal to 15mm is equal to 13μm.

The conductivity of PS in the frequency range ($100-10^6$ Hz) has been investigated for as prepared and annealed samples. Figure (3) shows the frequency dependence of ac conductivity σ(ω) for samples at room temperature (303K) and those which annealed at 373K, it is observed that according to the equation (2) the conductivity increases with the increase of frequency(ω):

$\sigma(\omega)=A\,\omega^s$ ....(2)

where A is the multiplicity factor, (*s)* is the exponent factor and ω is the angular frequency, in this case the conductivity is proportional to ω^s, where the exponent *(s)* is smaller than unity. From table (1) we notice that the values of s are constant with annealing temperature, where this behavior predicts that the transport mechanism of electrons is by tunneling in the potential barrier separating defects in the PS/Si structures [12].

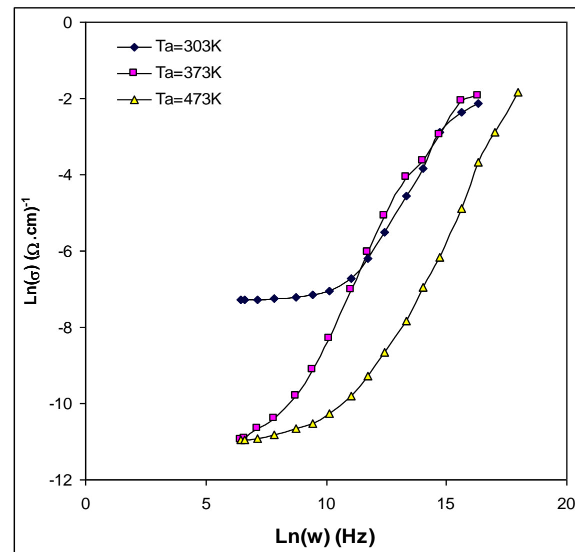


Fig.(3) The ac conductivity and angular frequency

The real ε_r and imaginary ε_i part of dielectric constant were calculated from the following [13]:

$\varepsilon_r=Ct/\varepsilon_0 A$ ....(3)

$\varepsilon_i=D\varepsilon_r$ ....(4)

Where C is the capacitance, ε_0 is the permittivity, A is an active area and D is the dielectric dispersion.

Representative plots of dielectric constant versus angular frequency (ω) at R.T and annealing temperature shown in figure (4).

These figures show that the dielectric constant decreases with the increase of angular frequency. A simple measure for the dielectric constant of semiconductors is the effective number of electrons per atom associated with a covalent bond. It directly contributes to the electronic polarization [14].

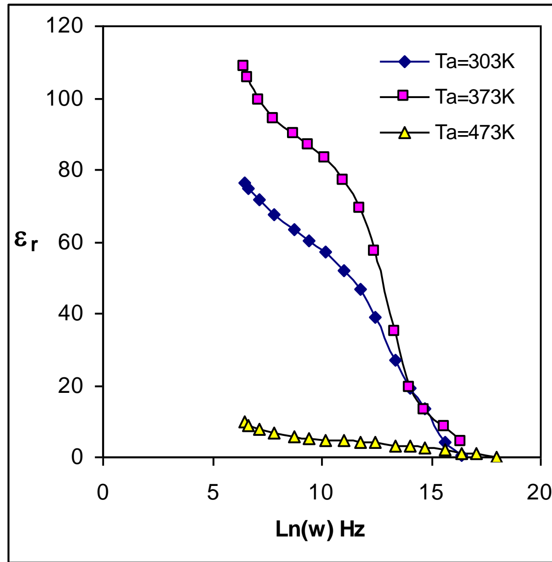


Fig.(4.a): The relation between real dielectric constant with angular frequency.

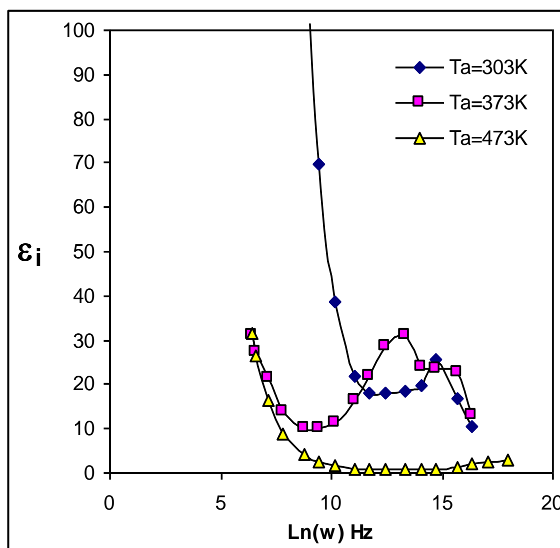
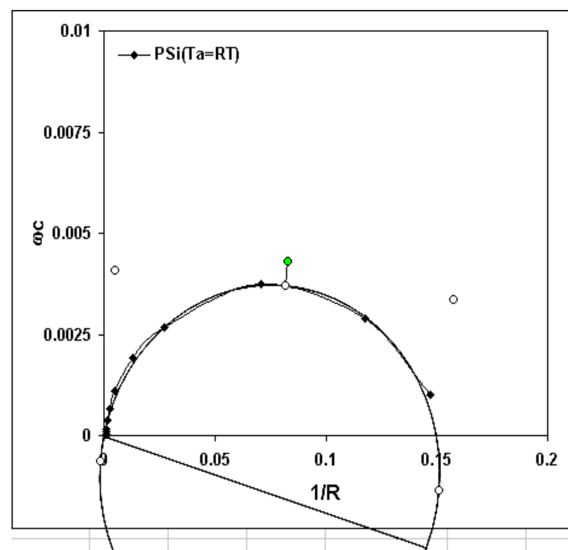


Fig.(4.b): The relation between imaginary dielectric constant with angular frequency

The polarizibility δ (dispersion parameter), which represents the angle between 1/R-axis and the diameter of semi-circle ($\theta=\delta\pi/2$), increases with annealing temperature[see as a sample fig.5].Microscopically, the electronic polarization reflects how strongly the population of valence is coupled with that of excited conduction electrons [15].

The relatively increased surface termination effects should also influence the dielectric response. As a result, the dielectric function of PS is greatly modified



Fig(5) The relation between 1/R and ωc.

Table (1) the value of the exponent s ,ε_s and α

T_a	S	ε_s	α
303	0.97	14.7	0.13
373	1.01	9.0	0.31
473	0.98	5.1	0.43

Porous Silicon layer capacitance

Capacitance measurements offer a valuable tool for investigating the electrical properties of porous silicon layers and devices containing porous silicon.

The capacitance of an Al/PS/p-Si has been studied as a function of bias voltage and frequency. Under reverse bias, the

capacitance is dominated by the heterojunction at the PS/bulk silicon interface. The slope of $1/C^2$ vs. bias corresponds to the doping density of the substrate (N_D).

The structures, which incorporate a porous silicon layer (PS), are often represented several capacitances and resistances (which represent distinct parts of the structure). For a structure with several capacitances in series, the total capacitance C_T is given by:

$$C_T= (1/ C_{ps}+\Sigma(1/C_i))^{-1} \ldots\ldots(5)$$

Where C_{ps} is the porous silicon capacitance and the C_i are the other capacitances of the interfaces near electrodes. It may be possible to obtain information on individual C_i by measuring C_T, e.g. as a function of frequency or applied bias.

The presence of PS has a significant effect on the measured values of total capacitance. In the most favorable cases, the porous Silicon capacitance (C_{ps}) itself may be deduced and dielectric constant of the porous silicon calculated.

It is found that metal/PS/Si structures behave like MIS structures.

For a small reverse bias, the heterojunction capacitance at the PS bulk silicon can be ignored.

C_{Si} is given by the Mott-Schottky expression [11]

$$1/(C_{Si}^2)=(2/e\varepsilon_0\varepsilon_{Si}N_D)[(V-V_{bi})-kT/e] \ldots.(6)$$

Where ε_0 is the permittivity of free space, ε_{Si} is the relative permittivity of silicon and N_D is the doping density of the substrate. Thus, a plot of $1/C^2$ against applied potential, gives a straight line with a slope related to N_D and an intercept represents of V_{bi}, the built in voltage.

Figures (6) show the relation $1/C^2$ vs. applied bias V. Table (2) illustrates the values of N_D,V_{bi} for PS sample and its annealed cases.

The capacitance at zero bias is proportional to the inverse of the PS thickness [16,17], Figures (7) show the relation between capacitance and reverse bias voltage .It can be calculate the capacitance(C_0) at zero bias [see table (2)] for PS samples at room temperature and those which have been annealed at T_a=373 and T_a=473K .

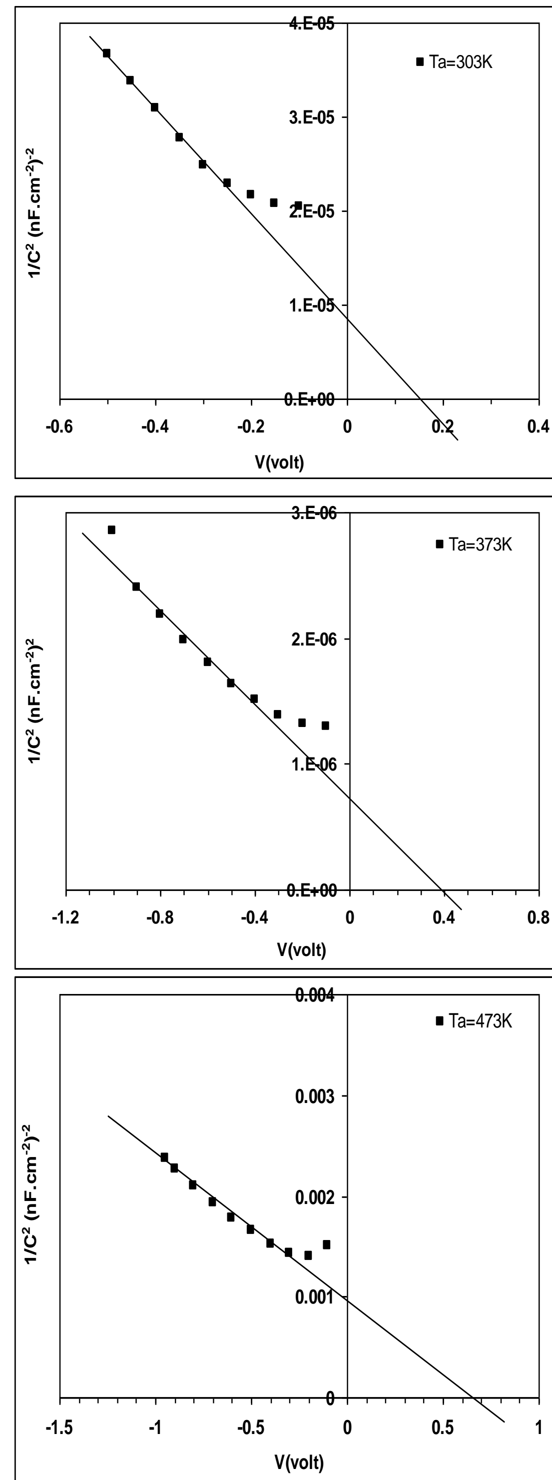


Fig.(6): V_{bi} for Al/PSi/Si/Al at (a)room temperature (b) T_a=373K (c) T_a=473K.

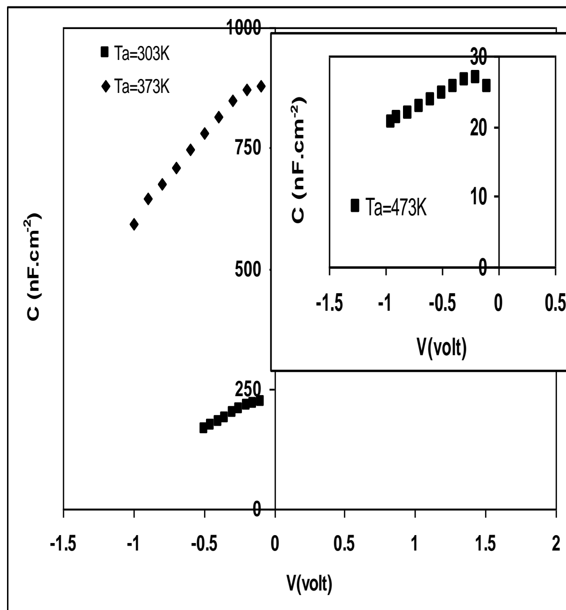


Fig.(7) The relation between capacitance vs. bias voltage at RT and different annealing temperatures

Table (2) the value of C_0, V_{bi} and N_D

T_a	C_0 ($nf.cm^{-2}$)	V_{bi} (eV)	N_D $(cm)^{-3}$
303	250	0.15	$1.97*10^{17}$
373	966	0.4	$5.93*10^{18}$
473	29	0.65	$7.91*10^{15}$

Conclusion

The sandwich structures Al/PS-(c-Si)/Al are prepared successfully, from the ac conductivity predict that the Quantum Mechanical Tunneling (QMT) mechanism is appropriate model for ac conductivity. Frequency dependence of capacitance shows that static dielectric constant decreases with annealing temperatures, and polarization increases with annealing process.

Applied bias dependence of capacitance shows that the built-in voltage increases with annealing process.

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