Structural and electrical properties of CdO/porous-Si heterojunction

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Abstract

The electrical properties of CdO/porous Si/c-Si heterojunction prepared by deposition of CdO layer on porous silicon synthesized by electrochemical etching were studied. The structural, optical, and electrical properties of CdO (50:50) thin film prepared by rapid thermal oxidation were examined. X-ray diffraction (XRD) results confirmed formation of nanostructured silicon layer the full width half maximum (FWHM) was increased after etching. The dark J-V characteristics of the heterojunction showed strong dependence on etching current density and etching time. The ideality factor and saturation current of the heterojunction were calculated from J-V under forward bias. C-V measurements confirmed that the prepared heterojunctions are abrupt type .The value of built-in-potential as function of etching current density was estimated.

Key words
Porous Si
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دراسة الخصائص الكهربائية للمفرق الهجيني CdO/porous Si/c-Si المصنع بطريقة التنميش الكيميائي

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الخلاصة

تم دراسة الخصائص الكهربائية للمفرق الهجيني من خلال ترسيب غشاء رقيق من اوكسيد الكادميوم على السليكون المسامي المحضر بطريقة التنميش الكهروكيميائي. تم دراسة الخصائص التركيبية والبصرية والكهربائية لغشاء اوكسيد الكادميوم المحضر بطريقة الاكسدة الحرارية السريعة.لقد اثبتت نتائج حيود الاشعة السينية ان السليكون المعالج كهروكيميائيا هو من النوع النانوي.اوضحت النتائج العملية ان خصائص تيار-جهد في حالة الظلام اعتمدت بشكل كبير على كثافة تيار وزمن التنميش الكهروكيميائي.مقدار عامل المثالية وتيار الاشباع كدالة لكثافة تيار التنميش تم حسابها من خصائص تيار–جهد في حالة الانحياز الامامي. لقد اوضحت خصائص سعة – جهد ان المفارق الهجينة هي من النوع الحاد وتم حساب جهد البناء الداخلي كدالة لظروف التحضير.

Introduction

Semiconductors have been used extensively in the area of circuit design and construction of electronic devices. The rapid change in electronics technology forced semiconductor research to obtain much smaller and faster semiconductors. Recently, visible light emission observed from porous silicon (PSi) structures obtained from single crystal silicon at room temperature has attracted intense attention and research. The interest partially fuelled by the indirect band gap and the ease with which silicon (Si) can be prepared. Porous silicon consists of a network of nanometer-sized silicon regions surrounded by void space [1]. In order to obtain p-Si with desired dimensions and working quantity, electrochemical methods were employed. Porous silicon was first obtained by Uhlir [2] and Turner [3] while studying electropolishing of Si in dilute HF acid solutions. Dimova [4] presented PS/c-Si solar cell fabricated by stain etching. The conversion efficiency increased to 30% after PS layer formation. Dhār and Chakrabarti [5] showed the feasibility of fabrication of high sensitive CdO/PS/Si heterojunction made by deposition of CdO on PS by chemical bath deposition. The dark current was very small (38nA at 20V) and the ratio of photocurrent to dark current was 1000. Timokhov *et al* [6] studied the electrical and photoelectrical properties of Al/PS/Si structure prepared by anodization at different current densities. The diffusion length of the minority charge carriers of the structures measured by the method of reverse photocurrent. Alwan [7] studied the optoelectronic properties of Al/PS/Si junction synthesized by anodization technique. He revealed that the figures of merit of the photodetectors are strongly dependent on anodization conditions. A. A. M. Farag in 2009 [8], had studied the structure and transport mechanisms of n-Si/PS heterojunction made by growing of n-Si layer by liquid phase epitaxial on porous Si layer prepared by anodization. The C-V measurements revealed that the junction is an abrupt type.

Ismail [9] studied the photosensitivity of Al/PS/Si /Al photodetector made by anodization technique with $50A/cm^2$ current density for 20min etching time. The responsivity obtained from such structure was 0.44A/W at 800nm and the response time was 100ns.

In this work, electrical, structural and morphological properties of CdO/porous Si/c-Si/Al heterojunctions made by electrochemical etching and rapid thermal oxidation are investigated.

Experimental Work

The mirror-like p-type (boron doped) of (111) orientation mono-crystalline silicon wafers with electrical resistivity of (14-22) Ω.cm and 500 ± 50 μm thick are used. The wafer scribed and cut into 1x1 cm^2 then cleaned carefully using acetone, ethanol, and demonized water (DI) to remove dirts and oil contaminations. After wards the wafer were cleaned for 5 minutes in each of the following: HNO_3, HCl, and hot DI to remove the room temperature native oxide layer SiO_2. Porous silicon was prepared by electrochemical etching (anodization) using an electrolyte containing 40% HF acid with several drop of ethanol to prevent bubbling for different current densities (10-40 mA/cm^2). The homemade [see Fig.1] electrochemical cell consist of the Si substrates set as anode and high purity Pt wire set as cathode (forward bias)

located inside Teflon container filled with electrolyte solution , power supply type was used provide electric field.

After etching the samples rinsed in deionized water and ethanol CdO thin film was deposited on porous silicon and clean glass substrate by rapid thermal oxidation (RTO) as technique as follows; high purity cadmium film (99.99%) provided from Aldrich co. was first deposited on Si using thermal evaporation technique under pressure down 10^{-5} torr.

The rapid thermal oxidation of the samples was performed using 650W halogen lamp .The oxidation is carried out in static air at temperature 550°C for 3 minutes. Fig.2 shows the schematic diagram of RTO system.

In order to measure the electrical properties of CdO thin film and CdO/Si, heterojunction, ohmic contacts were performed by evaporating of an aluminum film with purity of 99.99%. For CdO film deposited on glass substrate the ohmic contact was made through standard mask which is used for Hall measurement

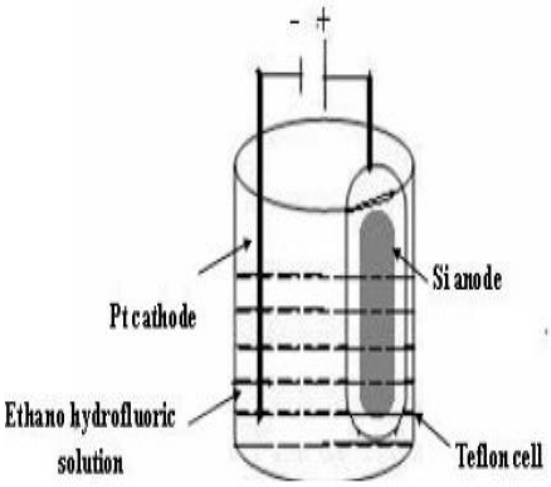

Fig.1:Schematic diagram of electrochemical anodization

The contacts were made on CdO/Si heterojunction by evaporating thin film (semitransparent) and thick of Al on front side (CdO) and back side (silicon), respectively. Spiral tungsten boat is used as source of evaporation. The evaporation process is carried out at a pressure of 10^{-5} torr using Edward Type. The cross-sectional view of CdO/PSi heterojunction photodetector was presented in Fig.3.

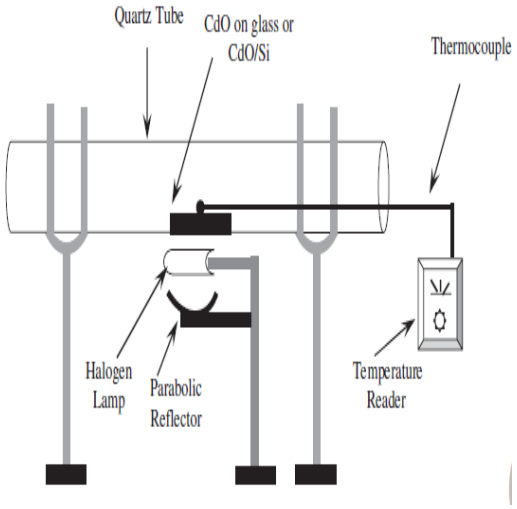

Fig.2: RTO system

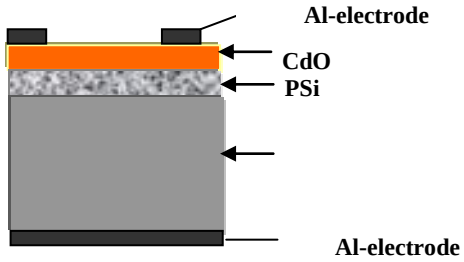

Fig.3:The CdO/PS/Si/Al sandwich heterojunction photodetector.

The direction of (111) plane for grown CdO film was calculated from Equation (1) below and found to be 4.68 Å of wurtzite structure [11].

$$\frac{1}{d^2}=\frac{4}{3}\frac{h^2+hk+l^2}{a^2}+\frac{l^2}{c^2} \qquad (1)$$

where d is the inter planar spacing, and (hkl) are the Miller indices. The calculated value of the lattice parameter are a=b=4.142, and c=6.724 Å.

This lattice constant was very close to that for ASTM powder diffraction data card number 05-640. No peaks belong to Cd or other phases were noticed in spectrum. The grain size G.S of the CdO film was estimated from Scherer's formula and found to be 60 nm. Fig.5 reveals the 2-D and 3-D AFM images of CdO films. These images show that the film is homogeneous and it has a large number of vertically aligned (columnar) grains. The scan area film for AFM analysis was 2x2μm^2. The surface was very smooth, the root mean square (RMS) of roughness was measured and found to be around 17.8 nm and (R_z) the ten point height was 111 nm. The average grain size of CdO film was measured from AFM analysis using software and found to be around 100 nm.

The Hall measurement revealed that the grown CdO film is n-type. The electrical resistivity at room temperature was 0.15Ω-cm and the Hall mobility of CdO film was about (25.5) cm^{2}V^{-1}s^{-1}.

Fig.6 shows current - voltage characteristics of CdO/Porous-Si under forward and reverse bias. The samples ($S_{10mA/cm^2\text{-}600s}$, $S_{20mA/cm^2\text{-}600s}$, $S_{30mA/cm^2\text{-}600s}$ and $S_{40mA/cm^2\text{-}600s}$) prepared with various current densities and constant etching time (600s). These figures, from J-V characteristics, show a clear rectification and indicate that the junction was anisotype junction. The current density voltage (J-V) characteristics for the forward bias are presented also on a semi-log plot.

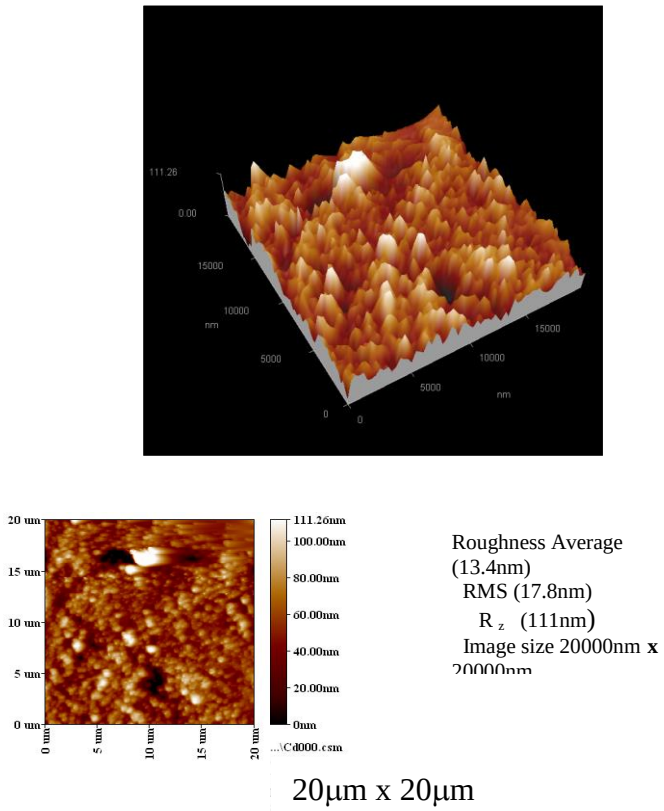

Fig. 5: 2D and 3D AFM images of CdO films.

All the figures reveal two distinct regions which belong to two different mechanisms of current transfer through the heterojunction with operational voltage ($V_T \cong 0.6\,V$). The first mechanism is localized at ($V_F < V_T$) where the recombination current is the dominant one. In this case, recombination process will taken place, that mean each excited electron from valance band to conduction band will recombine with a hole in valance band. For higher voltage $V_F > V_T$ there is another region where the tunneling current is predominant. In this region the bias voltage can deliver the electrons with enough energy to penetrate the barrier between the two sides of the junction. These results agree with other workers [12] for CdO/Porous-

Si prepared by electrochemical etching technique.

In reverse bias also there are two regions; first at low voltage, where the current increases with the applied voltage and the generation current is dominant. In second region the current independent from the voltage. One can also notice that the forward current decreases with increasing etching time, when etching time increases the porous layer increases and the porosity increases so the pore walls act as carrier trapped and cause high resistivity and the current will decrease [1].

The semi log (J-V) characteristics for the forward bias are presented in Fig.7. The forward current consists of two mechanisms. First mechanism represents a recombination current, second mechanism represents tunneling current. The mechanism of the forward current coincides to the tunneling-recombination mechanism. This result is agreed well with results of other workers [13] for CdO/PSi/Si photodetector prepared by electrochemical etching of (100) oriented p-type silicon wafer. The ideality factor (n) was calculated by equation (2), while the constant *A* is calculated from the following equation [14]:

$$A = d\ln(J_{f2}/J_{s2})/dV \qquad (2)$$

where J_{f2} is the forward current density for the tunneling region, J_{s2} is the saturation current density for this region. The ideality factor is given by [10]:

$$1/n = (kT/q)d\ln(J_{f2}/J_{s2})/dV \quad (3)$$

All figures of current-voltage characteristics shows the (J-V) characteristics of (CdO/Porous Si/Si/Al) hetreodetector at dark room temperature and under day light illumination of structure of Al thin layer deposited on to the mirror-like surface of the silicon substrate, the rectification properties of the structure is due to the formation of Shottky barrier between the Al thin film and the silicon substrate [15]. Several important parameters such as built in potential, junction capacitance, and doping concentration can be inferred from C-V measurements. Fig.8 demonstrates the variation of the junction capacitance versus reverse bias voltage. The Figure shows that junction capacitance varies inversely with reverse bias voltage. The distribution of (C-V) suggests that the junction of CdO/Porous Si/Si/Al is anisotype and analogous to the behavior predicted by the equation [16]:

$$\frac{C}{a} = \left[\frac{qN_nN_p\varepsilon_n\varepsilon_p}{2(\varepsilon_nN_n+\varepsilon_pN_p)(V_D-V_a)}\right]^{1/2} \qquad (4)$$

where the parameters are defined in [16]. Reduction of junction capacitance with increasing bias voltage is as a result of increasing built-in potential. Fig.8 shows the effect of etching current density on the junction capacitance. It is clear that the junction capacitance was a decreasing function with increasing etching current density. On the other hand, the junction capacitance increased with etching current density. This behavior was analogous to the C-V characteristics of the porous silicon fabricated by the electrochemical etching process [17, 18]. The capacitance of the structure dose not depends on the applied bias up to 5V. The current-voltage characteristics of the structure measured at bias voltage ± 5 volts showed that there was a strong in the junction. The forward current was fairly higher than the reverse current. This indicates that the barrier is formed in the structure, but they were not observed as shown the high value of V_{bi} calculated from Fig.9. This kind of behavior is agreement with that obtained by Zimin and Komarov [19] for thick layers and high porosity of the porous silicon prepared by electrochemical etching process. Fig.9 shows reciprocal of square

capacitance versus bias voltage ($1/C^2$-V). This plot shows a linear relationship C^{-2} with bias voltage indicates that the junction is an abrupt type; this means that the depletion layer is not constant and so the carrier concentration will be not constant at the depletion layer. This linear relationship represents the Schottky-like barrier between the Al layer and porous silicon. This behavior is similar to the many of the C-V characteristics of the porous silicon fabricated by the electrochemical etching process. Also built in potential (V_{bi}) can be calculated by extrapolating ($1/C^2$-V) plot to ($1/C^2$=0). The values of ideality factor (n) and saturation current density (J_s), calculated from J-V plots, in addition to the built - in potential V_{bi}, extracted from C-V plots, were listed in Table1 for CdO / Porous Si/Si/Al heterojunction

Table 1: Built-in Potential for CdO/Porous Si/Si/Al) Hetreodetector, current density saturation and ideality factor.

Samples	J_s (mA/cm^2)	***n***	V_{bi}(V)
S (10mA/cm^2-600s)	2µm	3.2	1.3
S (20mA/cm^2 -600s)	1.8µm	3.5	2.0
S (30mA/cm^2 -600s)	4µm	3.1	2.6
S (40mA/cm^2 -600s)	6.2µm	3.69	2.3

detector prepared at different current-density, different etching-time and listed in Table (1). There is a little fluctuation of the slope of ($1/C^2$) curve caused by the no uniformity of hetreodetector area.

Conclusions

- The structural and electrical properties of grown CdO are investigated. The electrical characteristics of heterojunction are strongly dependence on etching current density. The junction parameters are estimated as function of etching current density. The process used here is simple, cheep, reliable and promising.

- CdO prepared by RTO was polycrystalline and low resistive.

- This technique can be used to fabricate photodetectors and solar cell applications.

- I-V and C-V characteristics depend on the preparation conditions.

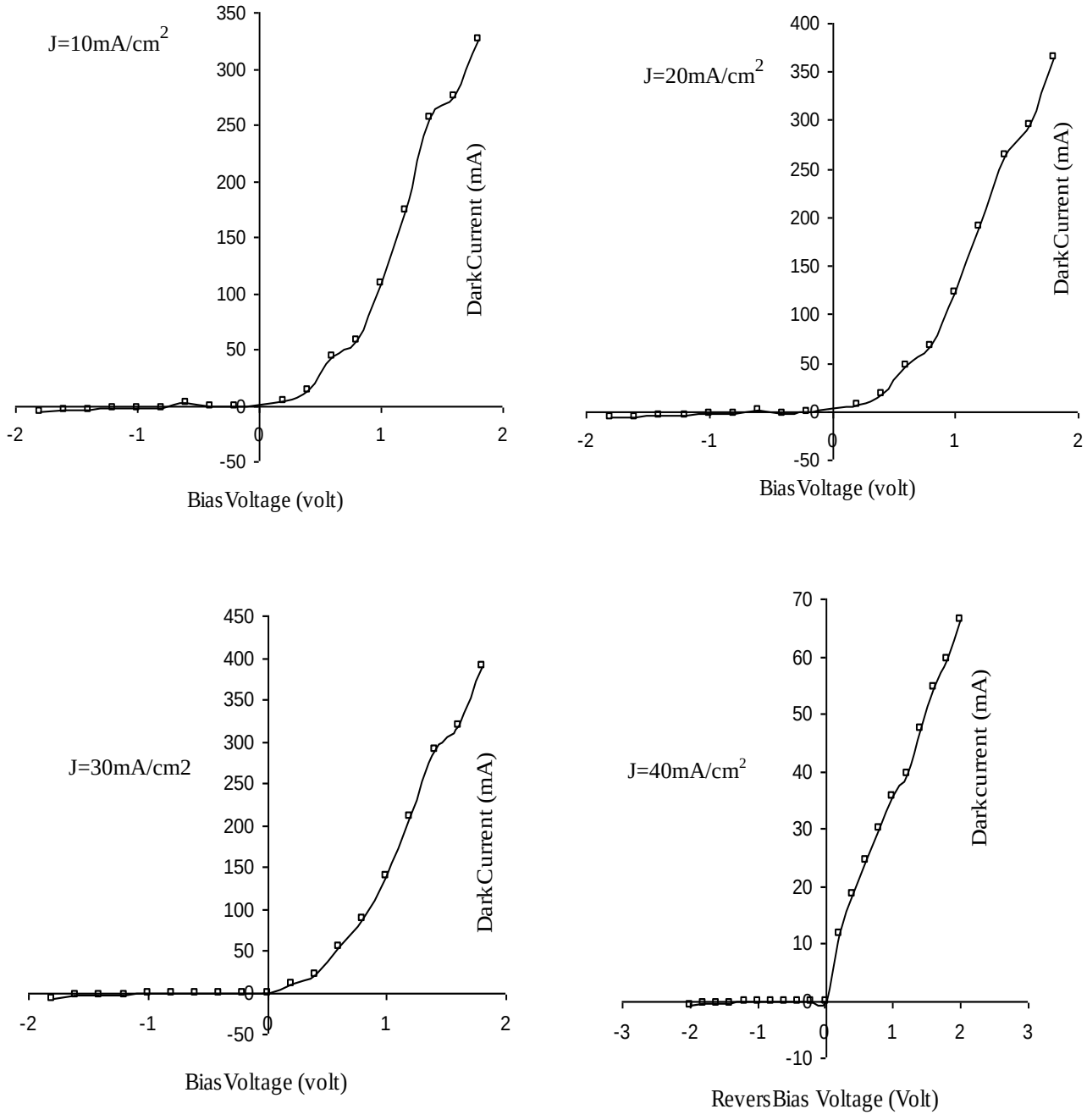

Fig. 6: I-V characteristics for CdO/Porous Si /Si/Al anisotype Heterojunctions at constant etching time.

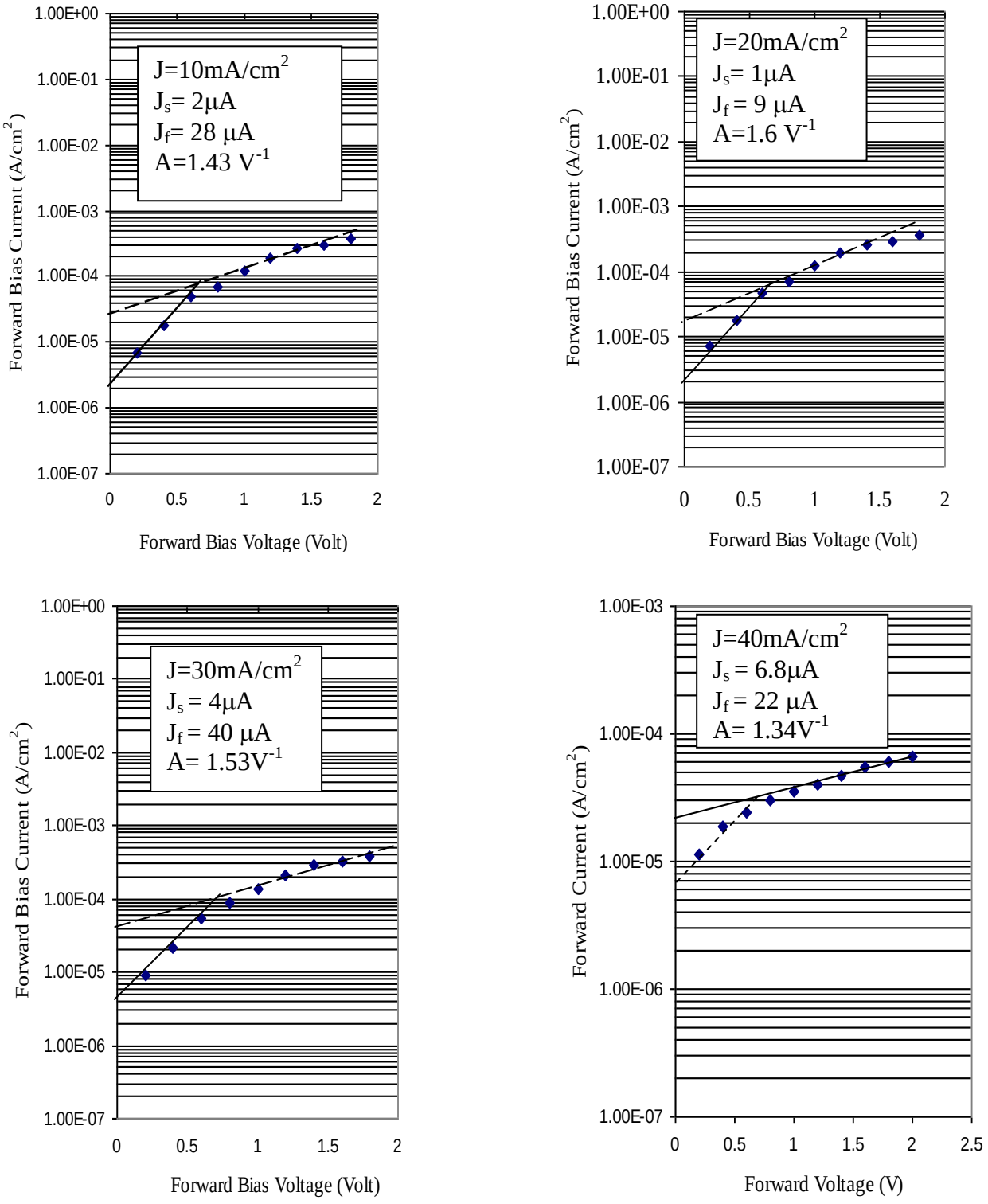

Fig.7: Forward J –V characteristics on a semi-log plot for CdO/Porous Si /Si/Al anisotype Heterojunctions at different etching current density.

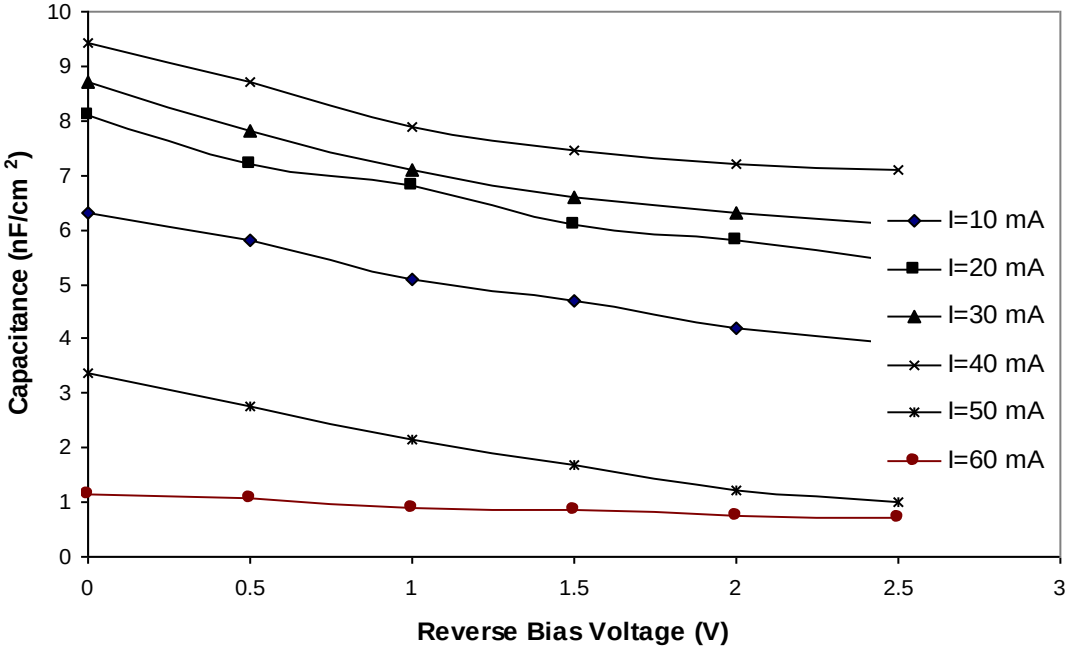

Fig.8: Capacitance-voltage characteristics for selective anisotype HJ detector.

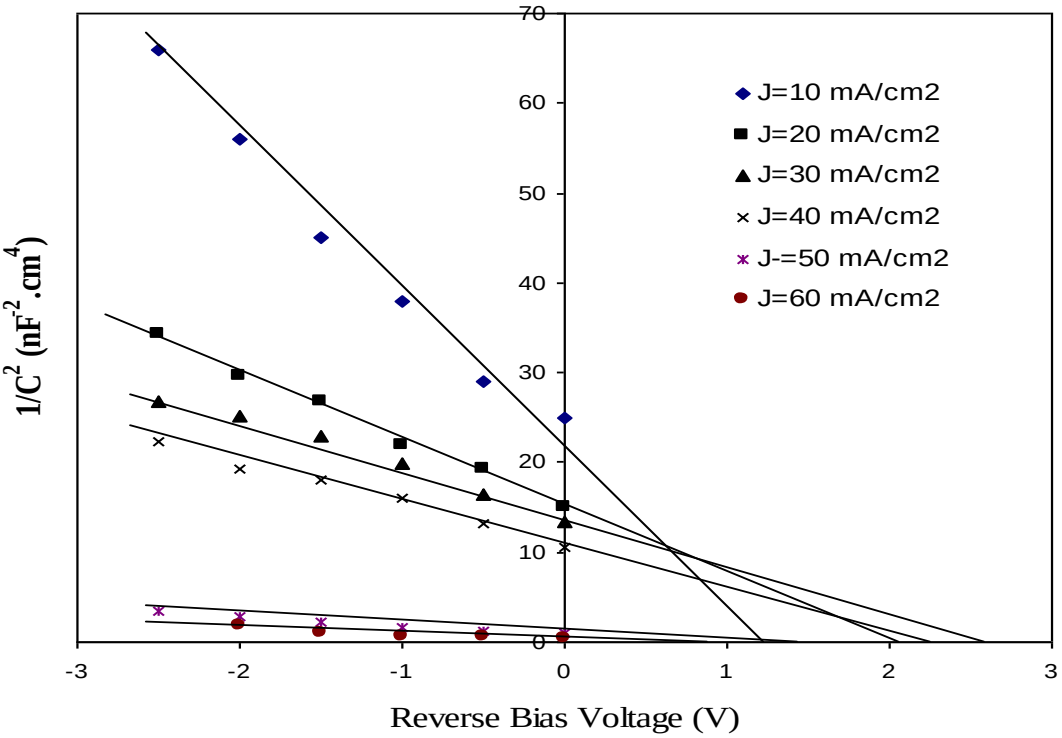

Fig.9: ($1/C^2$-V) Characteristics for (Al/CdO/Porous Si/Si/Al) HJ detector.

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