The effect of the etching time on the electrical properties of nano structure silicon

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Abstract

This work presents the study of the dark current density and the capacitance for porous silicon prepared by photo-electrochemical etching for n-type silicon with laser power density of 10mw/cm^2 and wavelength (650nm) under different anodization time (30,40,50,60) minute. The results obtained from this study shows different chara that different characteristic of porous diffecteristics for the different porous Silicon layers.

Key words
porous silicon,
etching,
nano structure

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تأثير زمن الحفر على الخواص الكهربائية للبناء النانوي للسيليكون

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الخلاصة

تمت دراسة كثافة التيار الكهربائي في غياب الاستضاءة والسعة الكهربائية لنماذج من السليكون المسامي المحضر بواسطة الحفر الضوئي الكهربائي الكيميائي للسليكون نوع n-type باستخدام كثافة قدرة ليزرية 10mW/ cm^2 وبطول موجي 650 نانوميتروبأزمان أنودة مختلفة (30,40,50,60) دقيقة والتي ستعطينا مميزات مختلفة لطبقات مسامية مختلفة.

Introduction

Since the discovery of visible photoluminescence on porous silicon (PS) at room temperature [1], a broad range of experimental and theoretical investigations have been kindled on this nano structural material [2].

The interest to study the electrical and photoelectrical properties of porous silicon layer appears first of all from prospects to developing of many technological applications such as detectors, solar cells, sensors,……etc[3].

The current-voltage characteristics, photovoltaic characteristics and the related electrical parameters such as ideality factor, rectification ratio and the charge carrier transport mechanisms metal/psi/C-Si/metal sandwich structure depend on the structural properties of(psi) layer[3,4,5]. However, less work has been done on electrical transport in porous silicon devices structures as compared to transport in porous silicon itself.

Moreover, these studies were mainly performed on devices structures with utilities from thick porous silicon layer when porous silicon properties significantly determine a conduction of the device [6].

Experimental Approach

Commercially available mirror-like n-type (100) oriented silicon wafer with resistivity (ρ=10Ω.cm) this silicon wafer has been cut off into small pieces as (1x1.5cm) this pieces was cleaned by (1:10) HF: ethanol and by using photo electrochemical etching with 48% concentration of HF.

Diode laser (10mw) with 650nm wavelength was used to illuminate the sample over area nearly (1x1cm). Photo-electrochemical etching was performed in mixture 48% HF and ethanol (1:1) at room temperature using (pt) electrode at various etching time (30, 40, 50, 60) minute.

After photo electrochemical etching process the samples were rinsed with dionized water and left in the environment for a few minute to dry and then stored in a plastic container filled with ethanol to prevent Oxidation.

by using thermal evaporation process in vacuum chamber Aluminum film was deposited on the back side of the samples and (3x3mm) area in the front side in order to creating an ohmic contact.

J-V characteristic was studied by using voltmeter, ammeter and power supply for forward and reverse bias of dark current and recorded for Al/psi/c-si/Al sandwich.

After photo electrochemical etching layer thickness (d) for Porous silicon and porosity (P) had been studied by using gravimetric measurements and using the equations [7]:

$$P = \frac{w_1 - w_2}{w_1 - w_3} \quad (1)$$

$$d = \frac{w_1 - w_3}{\rho s} \quad (2)$$

where w_1,w_2 is the weight of silicon sample before and after etching w_3 is the weight after porous silicon layer removed. ρ is the silicon density (2.3g/cm^3) and s (cm^2) the etched surface area.

Then the relation with duration time and power density was studied.

The relative permittivity of porous silicon was calculated by the relation [7]:

$$\varepsilon_{psi} = \varepsilon_{si} - p(\varepsilon_{si} - \varepsilon_{pore}) \quad (3)$$

where ε_{si} is relative permittivity of C-si and ε_{pore} is the relative permittivity of the air .

The capacity of porous silicon by using the relation [8]

$$C_{psi} = A * \varepsilon_{psi} * \varepsilon_o / d \quad (4)$$

where A is the area of porous silicon (area of etching) and ε_o is the permittivity of free space.

Results and Discussion

The electrical behavior of metal/psi/c-si/metal such as schottky or hetrojunction generally is determined depending on the characteristic of current-voltage curves.

Figs.1, 2, 3 and 4, show that the J-V characteristic of Al/psi/n-si/Al sandwich structure, which contains porous silicon layer prepared at (30,40,50,60) minute and power density (10mw/cm^2) of n-type substrate respectively, this figures demonstrate that the forward and reverse current densities at room temperature under dark as a function of the applied bias voltage for different etching times but with same power densities and with same wavelength.

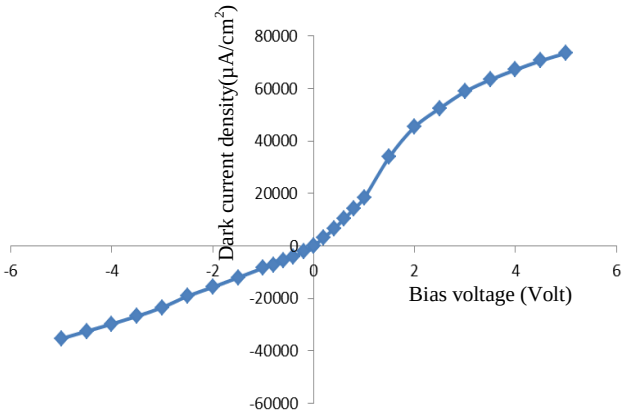

***Fig.1: J-V characteristic curve of (Al/Psi/n-Si/Al) of etching time (30* minute)**

Figs.1 and 2 show rectifying behavior and double current saturation which lead to the symmetrical characteristic and the current nearly have the same behavior for both bias voltage, the silicon substrate in the initial

time have porous silicon layer with low porosity and this lead to the semi homogenous layer with substrate of bulk silicon, but when it was increased the etching time means it was get small nano size and different electrical characteristic and this on the current density [6,9] .

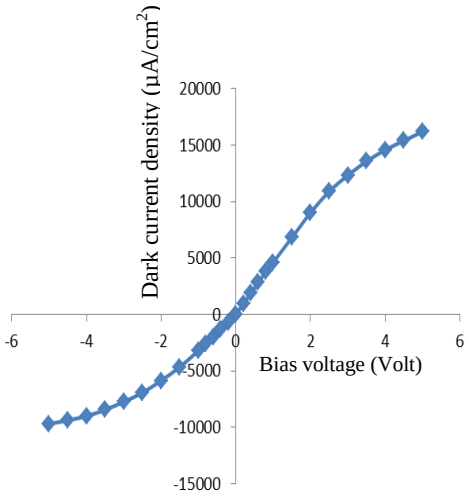

Fig.2: J-V characteristic curve of (Al/Psi/n-Si/Al) of etching time (40 minute)

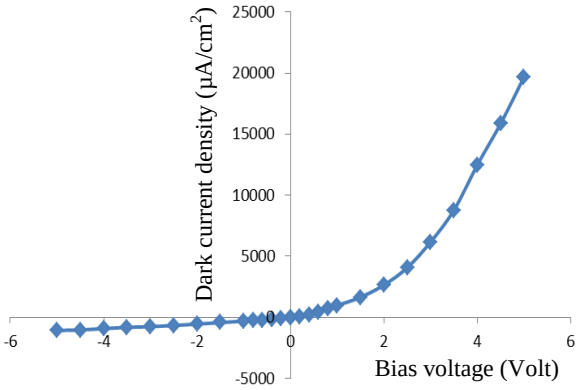

Fig.3: J-V characteristic curve of (Al/Psi/n-Si/Al) of etching time(50 minute

The good corresponding of our data with Milnes and Feucht model [10], and Ben-chorin*e* model [11]. Figs.3 and 4 illustrate behavior of J-V characteristic as Diode. The and which consist of various materials and this due to the longer etching time than that in the previous figures, The long etching time increases the current resistance of porous silicon. From Figs.3 and 4 it can be shown the current density value is less than in the previous figure. This result agrees with the (Schottky and hetrojunction model) [6].

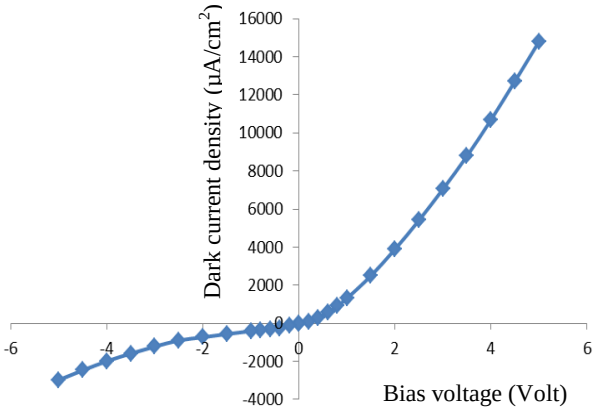

Fig.4: J-V characteristic curve of (Al/Psi/n-Si/Al) of etching time (60 minute)

Then one can conclude that the current density is decrease with increasing the etching time , which have different ideality factors and saturation region in J-V, our results are corresponds into many[12, 13,14]

Fig.5 shows the capacities of porous silicon layer as a function of etching time. It can be shows that for the initial time (30) minute the capacity of the porous silicon are nearly constant. This may be because the layer thickness of the porous silicon is slowly increased or nearly unchanged. However, when the etching time increased and the photo electrochemical etching process developed the depletion layer are the charge carriers depleted from the substrate silicon. The layer thickness of porous silicon are increased and the capacitance of porous silicon decreased [8,15].

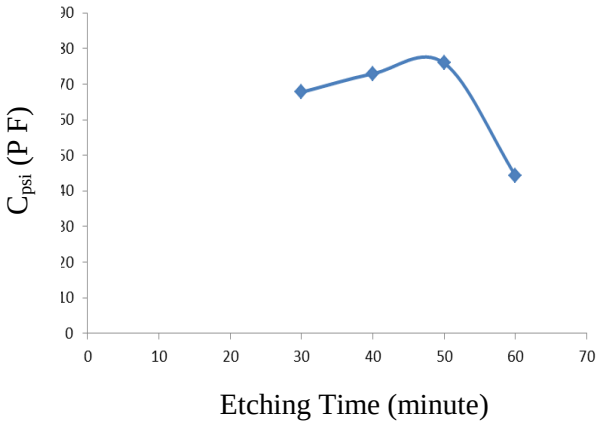

Fig.5: The capacitance of porous silicon function of time etching

Conclusions

From this work it can be concluded that the electrical properties of Al/psi/c-si/Al sandwich depends on the etching time andthis relate to the nano size of porous silicon and the various morphological of the porous silicon (porosity and layer thickness) causes increasing in the current resistance and this lead to different current density, on the other hand the capacity of porous silicon also related to the layer thickness of the porous silicon and nano size. From that we can get porous silicon layers with one layer or multilayers depending on the etching time and one can get ideal Diode by decrease the nanosize of silicon.

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